What is claimed is:

1. A substrate panel for use in semiconductor packaging, the substrate panel comprising:

a lead frame panel including a plurality of device areas, each device area having a die attach pad and a plurality of contacts, wherein each die attach pad includes a die support surface and a peripheral ledge that is recessed relative to the die support surface; and

a plurality of semiconductor dice, each die being attached to the die support surface of an associated die attach pad using an adhesive, wherein a portion of each semiconductor die extends beyond an outer edge of its associated die attach pad, and wherein the ledge is configured to retain an amount of the adhesive.

2. The substrate panel of claim 1 wherein the peripheral ledges extend around the outer edges of the die attach pads.

3. The substrate panel of claim 2 wherein each die attach pad has a second surface opposite to the die attach surface, wherein the area of the die attach surface is less than the area of the second surface.

4. A substrate panel as recited in claim 1 wherein bottom surfaces of the contacts are substantially co-planar with bottom surfaces of the die attach pads.

5. A substrate panel as recited in claim 4 further comprising an encapsulant applied to the lead frame panel, wherein the second surfaces of the die attach pads and the bottom surfaces of the contacts are exposed on an outer surface of the encapsulant, and wherein the peripheral ledges retain amounts of the adhesive so as to prevent the adhesive from being exposed on the outer surface of the encapsulant.

6. The substrate panel of claim 1 wherein at least some of the semiconductor dice are down bonded to the respective ledges of their associated die attach pads.

7. The substrate panel of claim 1 wherein the lead frame panel comprises a matrix of tie bars arranged in perpendicular rows and columns that define a two dimensional array of the device areas such that adjacent device areas are separated only by the tie bars.

8. A packaged integrated circuit, comprising:

a substrate having a die attach pad and a plurality of contacts, the die attach pad having an upper surface and a peripheral ledge proximate to the upper surface;

a semiconductor die mounted on the upper surface with an adhesive;

wherein a portion of the die extends beyond an outer edge of the upper surface; and

wherein the peripheral area is configured to retain a portion of the adhesive so as to inhibit a flow of the adhesive from the die attach pad.

9. The integrated circuit of claim 8 wherein the peripheral ledge is located proximate to, and surrounding, an outer edge of the upper surface.

10. The integrated circuit of claim 9 wherein the die attach pad has a lower surface opposite to the upper surface, the peripheral area located so that the area of the upper surface is less than the area of the lower surface.

11. The integrated circuit of claim 8 wherein bottom surfaces of the contacts are substantially co-planar with bottom surfaces of the die attach pad.

12. The integrated circuit of claim 11 further comprising an encapsulant applied to the substrate and the semiconductor die, wherein a lower surface of the die attach pad is exposed on an outer surface of the encapsulant, and wherein the peripheral ledge retains an amount of the adhesive so as to prevent the adhesive from being exposed on the outer surface of the encapsulant.

13. The integrated circuit of claim 8 wherein the die is down bonded to the peripheral area.

14. A method of attaching a semiconductor die to a lead-frame, comprising:

providing a lead-frame having a die attach pad, the die attach pad having an upper surface and a peripheral ledge proximate to the upper surface;

applying an adhesive to the upper surface of the die attach pad;

affixing a semiconductor die to the upper surface so as to displace a portion of the adhesive from the upper surface, and so that a portion of the semiconductor die extends beyond an outer edge of the upper surface; and

retaining the portion of the adhesive upon the peripheral ledge.

15. The method of claim 14 further comprising placing down bonds in electrical communication with the semiconductor die and the peripheral ledge.